



USER MANUAL

MINI EV-BOARD THETIS-I 2611109021011

VERSION 1.1

MAY 23, 2023

WURTH ELEKTRONIK MORE THAN YOU EXPECT

MUST READ

Check for firmware updates

Before using the product make sure you use the most recent firmware version, data sheet and user manual. This is especially important for Wireless Connectivity products that were not purchased directly from Würth Elektronik eiSos. A firmware update on these respective products may be required.

We strongly recommend to include in the customer system design, the possibility for a firmware update of the product.



Revision history

Manual version	HW version	Notes	Date
1.0	1.0	Initial version	March 2021
1.1	1.1	 Updated the values C2 and C12 values in the Hardware version 1.1 Updated Schematic. New corporate design. 	May 2023



Abbreviations

API Application Programming Interface ASCII American Standard Code For Information Interchange COG Chip on Glass COM Port Communication Port CSAP Configuration Service Access Point Configuration DSAP Data Service Access Point Data Service Access Data Service Data Service Access Data Service Access Point Data Service Access Point Data Service Access Point Data Service Access Point Data Data Service Access Point Data Data Data Service Access Point Data Data Data Data Data Data Data Da	Abbreviation	Name	Description
ASCII American Standard Code For Information Interchange COG Chip on Glass COM Port Communication Port CSAP Configuration Service Access Point Configuration DSAP Data Service Access Point UART control command for module configuration EV Evaluation ESD Electro Static Discharge FCC Federal Communications Commission FTDI Future Technology Devices International GND Ground Ground Input & Output JTAG Joint Test Action Group LDO Low Dropout LED Light Emitting Diode LFCLK Low frequency clock LFXO Low Signal level MCU Micro Controller Unit MSAP Management Service Access Point PCB Printed Circuit Board RF Radio frequency RSVD Reserved UART control command for module configuration UART control command for module wireless transmission.	API	Application Programming Interface	
COM Port Communication Port CSAP Configuration Service Access Point UART control command for module configuration DSAP Data Service Access Point UART control command for radio data transmission and reception EV Evaluation ESD Electro Static Discharge FCC Federal Communications Commission FTDI Future Technology Devices International Ground signal level that corresponds to 0 V HIGH High signal level IO Input & Output JTAG Joint Test Action Group LDO Low Dropout LED Light Emitting Diode LFCLK Low frequency clock LFXO Low frequency crystal oscillator LOW Low signal level MCU Micro Controller Unit MSAP Management Service Access Point PC Personal Computer PCB Printed Circuit Board RF Radio frequency RSVD Reserved UART control command for module wireless transmission.	ASCII	American Standard Code For	
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OTA Over the air PC Personal Computer PCB Printed Circuit Board RF Radio frequency Describes everything relating to the wireless transmission. RSVD Reserved	MSAP	_	
PC Personal Computer PCB Printed Circuit Board RF Radio frequency Describes everything relating to the wireless transmission. RSVD Reserved	NPO	Negative-Positive 0	
PCB Printed Circuit Board RF Radio frequency Describes everything relating to the wireless transmission. RSVD Reserved	OTA	Over the air	
RF Radio frequency Describes everything relating to the wireless transmission. RSVD Reserved	PC	Personal Computer	
RSVD Reserved wireless transmission.	PCB	Printed Circuit Board	
	RF	Radio frequency	
SMA SubMiniature version A	RSVD	Reserved	
	SMA	SubMiniature version A	

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SMD	Surface-Mount Device	
SWD	Serial Wire Debug	
THT	Through-hole technology	
TTL	Transistor-Transistor Logic	
UART	Universal Asynchronous Receiver Transmitter	Universal Asynchronous Receiver Transmitter allows communicating with the module of a specific interface.
USB	Universal Serial Bus	
VDD	Voltage Drain Drain	Supply voltage
WE	Würth Elektronik	

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1 Supported radio modules

The evaluation board described in this manual is exclusively for the Thetis-I module:

Order code	Product Name	Description
2611011021010	Thetis-I	Wirepas Mesh 2.4 GHz radio module with smart antenna configuration

Order code	Product Name
2611109021011	Mini EV Board Thetis-I

Table 1: Compatibility

Content 2611109021011	Quantity
Thetis-I mini evaluation board	1
Packaging: ESD safe cover	1

Table 2: Content Thetis-I Wirepas Mini EV Board



2 Functional description

Mini EV-Board Thetis-I is an application-oriented development board meant to support the rapid prototyping of a Wirepas mesh network. It offers the user the possibility to develop hardware and software for the Thetis-I radio module.

By default, the basic pin headers and connectors are assembled in the mini evaluation board. The additional components shall be assembled by the user according to requirements and application.

The additional assembly is intended for experienced developers, as additional accessories and basic soldering skills are necessary to take the board into operation.

Accessories required:

- · Additional assembly components listed in the table 4.
- Soldering equipment
- (Optional) TTL-232R-3V3 FTDI cable

For the connection to a micro controller or PC the evaluation board is equipped with P3 Pin header which is connected to the pins of the radio module. The additional pin headers can be soldered to the placeholders to access the module pins. Jumpers allow the power selection and current measurement of the module.

The mini evaluation board can be connected to an USB port of a PC using TTL-232R-3V3 FTDI cable.

2.1 Taking into operation - PC

To take the mini evaluation board into operation using a PC, pin header P3 shall be used. The corresponding FTDI driver package (www.ftdichip.com/Drivers/VCP.htm) has to be installed on the PC. The installation guidelines shall be followed: (https://www.ftdichip.com/Support/Documents/InstallGuides.htm)

To take the mini evaluation board into operation, please perform the following steps:

- 1. Connect the evaluation board to the PC
 - a) Connect the TTL-232R-3V3 FTDI cable to the connector P3 of the evaluation board.



Incorrect orientation of TTL-232R-3V3 FTDI cable will damage the radio module.



- b) Then connect TTL-232R-3V3 FTDI cable to the USB port of the PC. In that way a COM port can be detected and installed on the PC. In the device manager the COM port name of the TTL-232R-3V3 FTDI cable can be found. A COM port shall appear for example: "COM12" in Windows systems or "/dev/ttyUSB0" in Linux systems.
- 2. Configure the mini evaluation board as sink
 - a) Open the Wirepas Commander PC tool, available for free download at this page: https://we-online.de/wcs-software
 - b) Select the right COM port of the Thetis-I evaluation board and press the "Open/Close COM port" button.

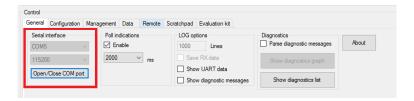


Figure 1: Open COM port

- c) Configure the connected Thetis-I evaluation board as sink of the network: go to the "Configuration" tab and set
 - the node address to a unique address.
 - the address of the network to 7.
 - the channel of the network to 39.
 - the node role to "SINK".

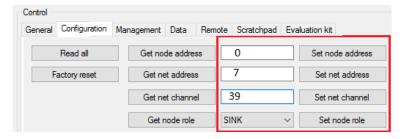


Figure 2: Configure the sink

d) Start the radio stack on the "Management" tab.



Figure 3: Start the sink

3. To make other Mini EV-Board Thetis-I mini evaluation board units join this Wirepas network, connect them to the PC in the same way.



- 4. Configure these mini evaluation boards as routing nodes taking part in the Wirepas network consisting of the previously configured sink device.
 - a) Open further instances of the Wirepas Commander.
 - b) Select the right COM port of the Thetis-I evaluation board and press the "Open/Close COM port" button (see figure 1).
 - c) Configure the connected Thetis-I mini evaluation boards: go to the "Configuration" tab and set
 - the node address to a unique address (for the sink we used 0 in the example, thus do not use 0 here for the routing node).
 - the address of the network to 7.
 - the channel of the network to 39.
 - the node role to "ROUTER_NODE".
 - d) Start the radio stack on the "Management" tab (see figure 3).
 - e) To transmit data from the Wirepas mini evaluation board to the sink enter the data you want to transmit in the fields of the "Data" tab. As destination node address type "sink".

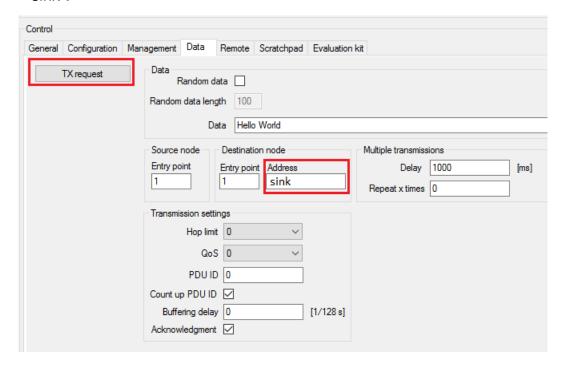


Figure 4: Transmit data to the sink

All details about the UART interface can be found in the Wirepas dual MCU manual [1] and the Mini EV-Board Thetis-I manual.

2.2 Taking into operation - Host controller

To take the mini evaluation board into operation using a host controller, pin header P3 shall be used.

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An external power supply shall be connected to the evaluation board. The power supply option 2 or 3 from the table 15 shall be used. It is important that the VDD is stable and able to reliably supply the module's static and peak current consumption as specified by the module manual.

The next step is to connect the communication lines of the module to the host controller. The headers P1, P2 and P3 can be used to connect the module pins to the host.

All details about the UART interface can be found in the Wirepas dual MCU manual [1] and the Mini EV-Board Thetis-I manual. A free C implementation of the Wirepas Dual MCU API is available at: https://github.com/wirepas/c-mesh-api.



3 Development board - Thetis-I mini evaluation board

3.1 Block diagram

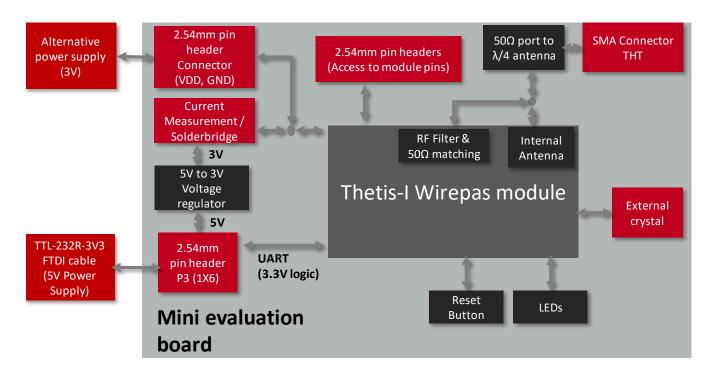


Figure 5: Block diagram



3.2 Connectors and pin headers

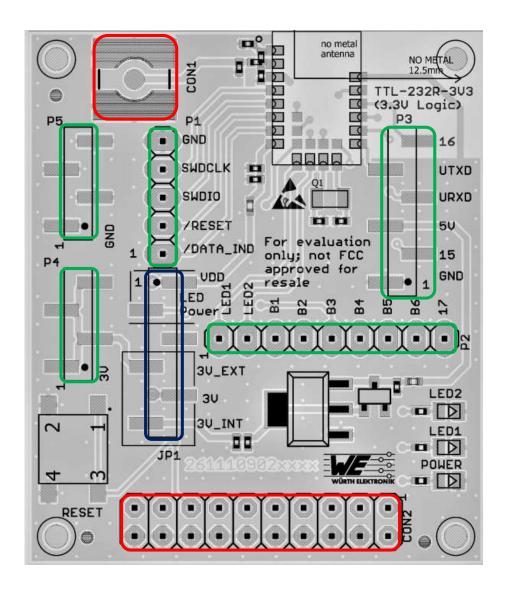


Figure 6: Connectors and pin headers

The table 3 lists the pin headers assembled on the evaluation board by default. All the components listed in the table 3 are SMD components.

Pin header	Function	Pins	WE article number
P3	TTL-232R-3V3 FTDI cable connection / Access to module pins	1X6	61000618321
P5	External power supply GND	1X4	61000418321
P4	External power supply 3V	1X4	61000418321
JP1	Power supply selection	1X6	61000618321

Table 3: Default assembled connectors



The table 4 lists the optional components for the evaluation board. Most of the components are common THT components that can be soldered on manually by the user.

Placeholder	Function	Pins	WE article number
P1	Module access pins	1X5	61300511121
P2	Module access pins	1X9	61300911121
CON1	SMA Connector	SMD	60312102114405
CON2	JTAG Connector	2X10	61302021121

Table 4: Additional assembly components



Based on the necessity the optional components shall be assembled.



Holes with 2mm diameter on all the four corners are available for spacer or standoff connections

3.2.1 P1, P2, P3: Module access pins

P1	nRF52840	Function
1	P0.02	/DATA_IND
2	P0.18	RESET
3	SWDIO	SWDIO
4	SWCLK	SWCLK
5		GND

Table 5: Pin header P1



P2	nRF52840	Function
1	P0.19	LED1
2	P0.22	LED2
3	P0.09	B1, RSVD
4	P0.10	B2, RSVD
5	P0.23	B3, RSVD
6	P1.00	B4, RSVD
7	P0.21	B5, RSVD
8	P0.07	B6, RSVD
9	P0.03	17, RSVD

Table 6: Pin header P2

3.2.2 P3: TTL-232R-3V3 FTDI cable connector

P3	nRF52840	Function
1		GND
2	P0.11	15, RSVD
3		5 V
4	P1.09	URXD
5	P1.08	UTXD
6	P0.12	16, RSVD

Table 7: Pin header P3



Pin header P3 is used to connect the TTL-232R-3V3 FTDI cable. P3 can also be used for direct host connection.



3.2.3 P4, P5: Alternative power supply connection

P4	Connection
1,2,3,4	3V External power supply

Table 8: Pin header P4

P5	Connection
1,2,3,4	GND

Table 9: Pin header P5

All the information related to the power supply are described in the chapter 3.5.1.

3.2.4 JTAG Debugging Interface

JTAG Pin	Function	JTAG Pin	Function
1	VDD	2	Not connected
3	Not connected	4	GND
5	Not connected	6	GND
7	SWDIO	8	GND
9	SWCLK	10	GND
11	Not connected	12	GND
13	Not connected	14	GND
15	RESET	16	GND
17	Not connected	18	GND
19	Not connected	20	GND

Table 10: JTAG debugging interface

3.2.5 SMA

In order to use an external antenna, the SMA connector and relevant capacitors shall be assembled. The 2.4GHz antenna Himalia from Würth Elektronik eiSos (order code 2600130021) is a perfect match: https://www.we-online.de/katalog/en/WIRL_ACCE_2600130021



By default the internal PCB antenna of the module is used.



SMA	Connection
Inner	Module RF pin
Outer	GND

Table 11: Pin header SMA



In order to use an external SMA antenna, 22 pF capacitor (0402) on position C1 shall be assembled. C2, C8, C11 and C12 should be left unpopulated.



Optional: Experts have the possibility to use C11, C1 and C8 for additional filtering or fine tuning.

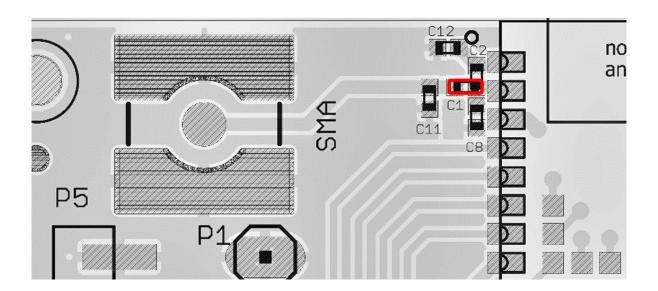


Figure 7: Capacitor connection to external antenna



In order to use the internal PCB antenna of the module, a 22 pF capacitor (0402) on position C2 shall be assembled. C1, C8, C11 and C12 should be left unpopulated.



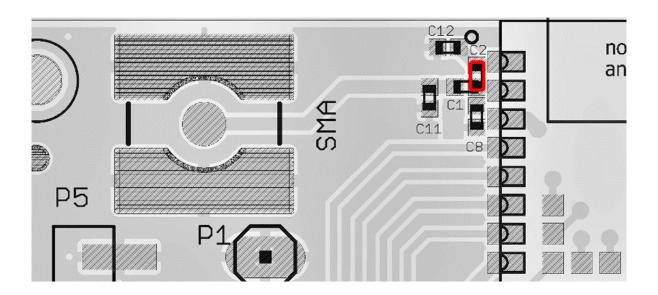


Figure 8: Capacitor connection to internal antenna



Optional: Experts have the possibility to use C2, C8 and C12 for additional filtering or fine tuning.



3.3 Jumpers

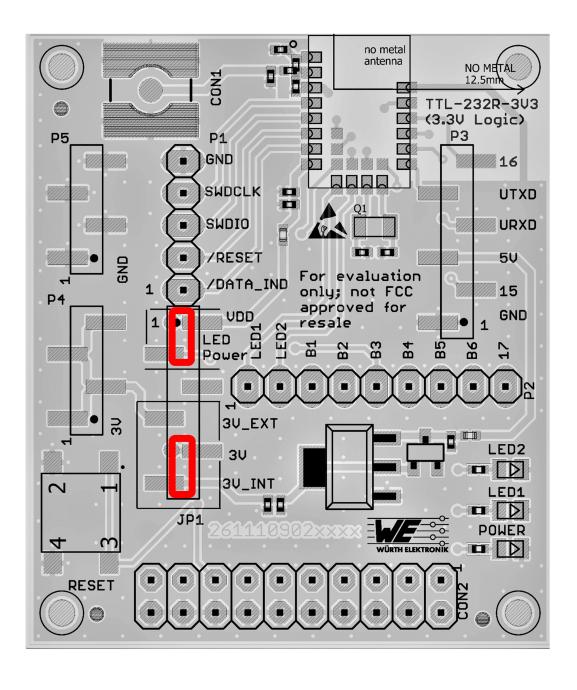


Figure 9: Jumpers



3.3.1 JP1

JP1 pin header is assembled by default.

JP1	Function
1	VDD
2	LED Power
3	Not connected
4	3V LDO Output
5	VDD
6	3V External Power supply

Table 12: Pin header JP1

3.3.1.1 JP1: Power LED separation

JP1	Function	Jumper set(default)
1<->2	Power LED sourced by VDD	Yes

Table 13: Pin header JP1 Power LED

3.3.1.2 JP1: Power supply selection

JP1 shall be set to choose either internal on-board LDO or the external 3V as power supply.



The power LED is connected to the VDD line by the 1-2 pins of JP1. To measure module current consumption, the jumper JP1 (1<->2 pins) shall be removed.

JP1	Function	Jumper set(default)
4<->5	External 3V power supply	No
5<->6	Internal LDO power supply	Yes

Table 14: Pin header JP1 Power supply selection



On JP1 a current meter shall be connected instead of a jumper to measure the current consumption of the module.



3.4 Reset button

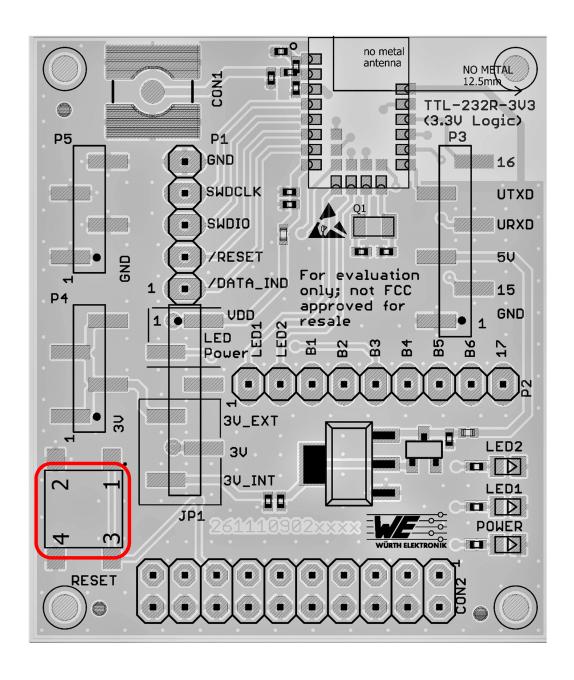


Figure 10: Buttons

On IC level the active low reset input is configured with a pull up resistor. The module provides a /RESET pin that is connected to this button so that the module can be restarted properly.



3.5 Function blocks

3.5.1 Power supply

The mini evaluation board can be powered either by TTL-232R-3V3 cable or by an external power supply. The table 15 lists the connection for different power supply options.

No	Power supply	Connector	JP1 Jumper
1	TTL-232R-3V3 cable	P3	Pin (5<->6)
2	External supply	P3 Pin-3 (5 V) P3 Pin-1 (GND)	Pin (4<->5)
3	External supply	P4 (3V) and P5 (GND)	Pin (4<->5)

Table 15: Power supply option

3.5.1.1 Connector P3, power supply through TTL-232R-3V3

The evaluation board can be sourced by TTL-232R-3V3 cable through P3 connector. The TTL-232R-3V3 cable powers the board with 5 V supply. The integrated voltage regulator regulates the connected voltage 5 V down to 3 V and supplies the remaining parts of the circuit. If the module is sourced, the *Power LED* lights up.

3.5.1.2 Connector P3, power supply through external source

The evaluation board can be sourced by an external power supply through the P3 connector Pin-3 (5 V) and P3 Pin-1 (GND). If the module is sourced, the power *Power LED* lights up.

3.5.1.3 Connectors P4 and P5, power supply through external source

The development board can be sourced by an external power supply through the P4 (1.9-3.6 V) and P5 (GND) connector. If the module is sourced, the *Power LED* lights up.

3.5.2 **UART / USB**

The TTL-232R-3V3 cable is used for USB/UART connection between PC and the evaluation board. The IO level of the TTL-232R-3V3 cable is 3.3 V. Using the FTDI-driver the PC will show a virtual COM port which can be used to communicate with the module.

3.5.3 UART direct

P3 connector shall be used for host connection. The UART of the host can be directly connected to P3 (pins are labelled on the evaluation board). The module RXD line must be handled accordingly by your host (i.e. pulled up while inactive and during module boot-up).



Beware of IO level compatibility. The host must obey the values stated in the module's manual. Especially the IO level restrictions must be implemented by a host system (i.e. using a level shifter to use the allowed IO levels).

3.5.4 LFXO crystal

For higher LFCLK accuracy (better than ±250 ppm) a low frequency crystal oscillator of 32.768 kHz (LFXO) shall be used. A crystal, 3.2 ×1.6 mm package, order code *830009706* with capacitors C9 (12 pF) and C10 (12 pF), 0402 package is used in the reference design.

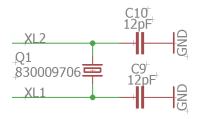


Figure 11: LFXO

Depending on parasitic capacitance of PCB, the capacitance value of C9 and C10 shall be calculated.

nRF52840 pin P0.00/XL1 and P0.01/XL12 are connected to module pad XL1 and XL2 respectively.

The input capacitance of the pad XL1 and XL2 are 4 pF. The values of C9 and C10 can be calculated as follows.

The load capacitance of LFXO is given by

$$C_l = \frac{C9_l * C10_l}{C9_l + C10_l} \tag{1}$$

If $C9_l = C10_l = C$, then

$$C_l = \frac{C}{2} \tag{2}$$

whereas,

$$C9 = C - C_{XL1} - C_{PCB} (3)$$

$$C10 = C - C_{XL2} - C_{PCB} (4)$$

 C_l = Load capacitance of LFXO crystal.

 C_{XL1} = Input capacitance of Pad XL1 (4 pF)

 C_{XL2} = Input capacitance of Pad XL2 (4 pF)

 C_{PCB} = Parasitic capacitance of PCB

Parasitic capacitance of the PCB can vary depending on design and track length. Typical values for parasitic capacitors range from 0.5 pF to 2 pF.

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For the crystal *830009706* with load capacitance of 9 pF and parasitic capacitance of 2 pF (for the Thetis-I Mini EV board), the value of C9 and C10 results in 12 pF, which was also tested on the Thetis-I Mini EV board.



3.5.4.1 LFXO Design guidelines

- 1. LFXO shall be placed away from high frequency components and traces.
- 2. The ground connection for the load capacitor shall be short using ground vias.
- 3. The crystal shall be placed close to the module.
- 4. PCB traces between module and the crystal shall be kept short.
- 5. Load capacitors shall be low leakage and temperature stable (NPO or COG) type.
- 6. The differential traces shall be kept to the same length.
- 7. Ground area shall be placed under the crystal and connected to the main ground plane.
- 8. Open traces to the pins shall be avoided to reduce parasitic capacitance and coupling effects.
- 9. Ground area shall be used between the crystal traces and other PCB traces for better decoupling.

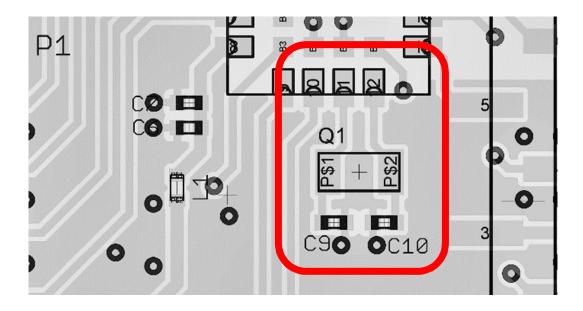


Figure 12: LFXO assembly

3.5.5 Programming interface

The evaluation board provides a place holder for 2×10 pin connector CON2. It can be used to connect directly to a JTAG flash adapter used for development. Please take care of the correct mounting of the flash adapter. The recommended flash adapter is one of the "Segger J-Link" family.



3.6 Schematic

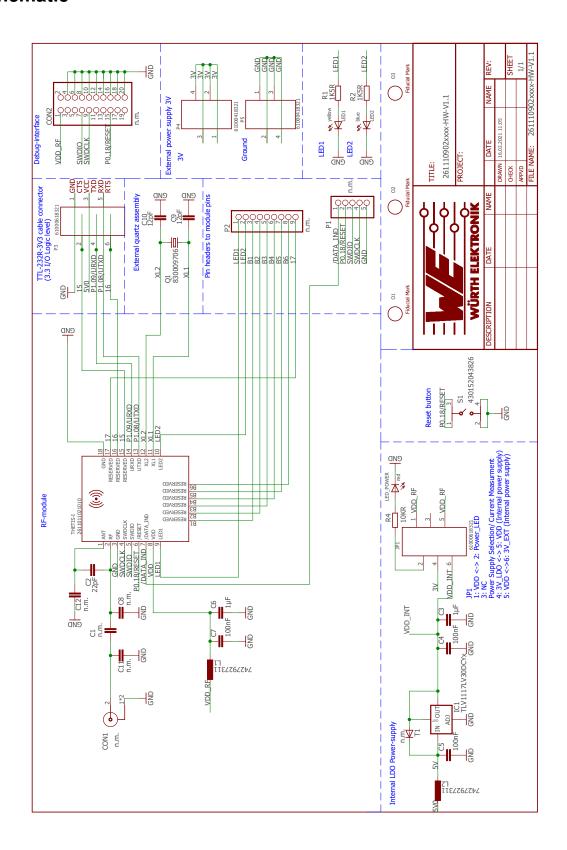


Figure 13: Schematic sheet



3.7 Layout

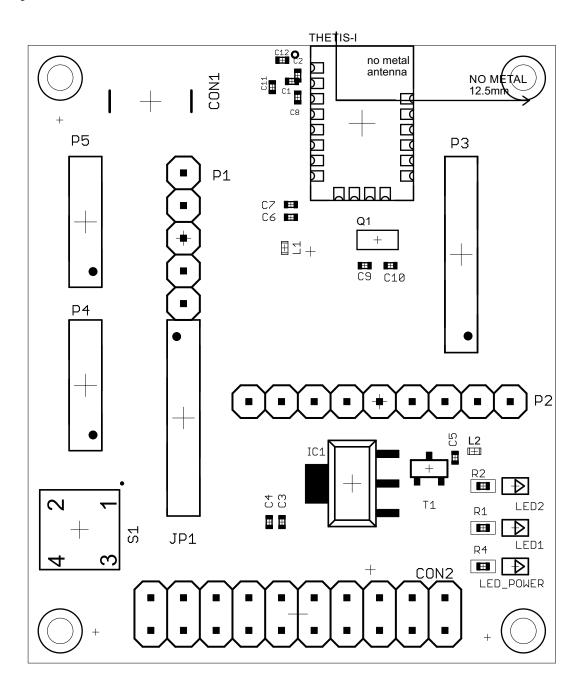
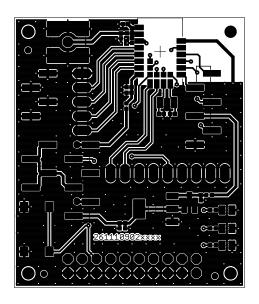
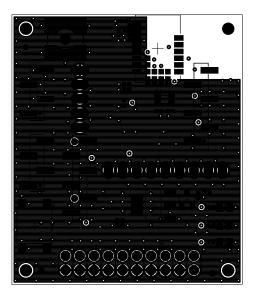
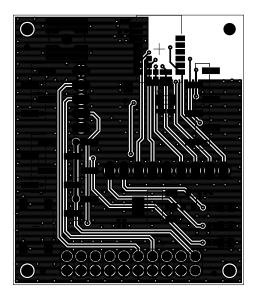


Figure 14: Assembly









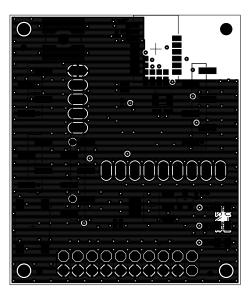


Figure 15: Top, bottom & internal layers



3.8 Bill of materials

Part	Value	PACK	MANUFACTURER	NR
C1	n.m.	0402		
C2	22pF	0.5mm	Würth Elektronik	885012005027
C3	1μF	0402	Würth Elektronik	885012105012
C4	100nF	0402	Würth Elektronik	885012205037
C5	100nF	0402	Würth Elektronik	885012205037
C6	1μF	0402	Würth Elektronik	885012105012
C7	100nF	0402	Würth Elektronik	885012205037
C8	n.m.	0402		
C9	12pF	0402		
C10	12pF	0402		
C11	n.m.	0402		
C12	n.m.	0402		
CON1	n.m.	SMD		
CON2	n.m.			
IC1	LDO, 3V		0	
JP1	61000618321	SMD	Würth Elektronik	61000618321
L1	7427927311	0402	Würth Elektronik	7427927311
L2	7427927311	0402	Würth Elektronik	7427927311
LED1	yellow	0805	Würth Elektronik	150080YS75000
LED2	blue	0805	Würth Elektronik	150080BS75000
LED_POWER	red	0805	Würth Elektronik	150080RS75000
01	OPT_MARKE		0	
O2	OPT_MARKE			
O3	OPT_MARKE			
P1	n.m.		0	
P2	n.m.			
P3	61000618321	SMT	Würth Elektronik	61000618321
P4	61000418321	SMT	Würth Elektronik	61000418321
P5	61000418321	SMT	Würth Elektronik	61000418321
Q1	830009706	3.2 x 1.5mm S	Würth Elektronik	830009706
R1	1K5R			
R2	1K5R			
R4	10KR			
S1	430152043826		Würth Elektronik	430152043826
T1	n.m.			
THETIS-I	2611011021010	SMD	Würth Elektronik	2611011021010

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4 References

[1] Wirepas. Wirepas Mesh Dual-MCU API Reference Manual, WP-RM-100, version 5.1A. https://www.we-online.com/Man/WIREPAS-I.



5 Regulatory compliance information

5.1 European Conformity

Pursuant to Article 1 (2.) of the EU directive 2014/53/EU, Article 1 (2.) the directive does not apply to equipment listed in Annex I (4.): custom-built evaluation kits designed for professionals to be used solely at research and development facilities for such purposes.

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